Method of manufacturing a semiconductor device with a bipolar transistor and device with a bipolar transistor

The invention relates to a method of manufacturing a semiconductor device comprising a semiconductor body of silicon with a bipolar transistor including a base, an emitter and a collector, wherein the emitter is formed in a first region of the semiconductor body and wherein an electrically insulating layer is formed on the semiconductor body in which a window is formed in the first region of the semiconductor body and a semiconductor layer of silicon is deposited on the insulating layer which fills the window in the insulating layer and which extends laterally over the insulating layer along the window and after the deposition of the semiconductor layer, the semiconductor layer and the insulating layer are removed in a second region of the semiconductor body which borders the first region which is covered by a stack comprising a remaining part of the insulating layer and a remaining part of the semiconductor layer and hereinafter a metal layer is deposited on top of the remaining part of the semiconductor layer and on the second region of the semiconductor body of silicon and a silicide is formed between the metal layer and the second region of the semiconductor body of silicon and between the metal layer and the remaining part of the semiconductor layer of silicon, and wherein a side face of the stack is provided with means to avoid bridging of the silicides to be formed. With this method both discrete and integrated bipolar transistors can be made having excellent electrical properties like high speed and low dissipation.

Such a method is known from United States patent application US 2002/0102787, published on August 1 2002. In said document, a description is given of a method in which a SiGe heterojunction bipolar transistor is made with an emitter formed on a SiGe base and wherein the sidewalls of the emitter are protected by a conformal passivation layer. The conformal passivation layer is formed on the exposed sidewalls of said emitter prior to siliciding the structure. The presence of the passivation layer in the structure prevents silicide short from occurring by eliminating bridging between adjacent silicide regions; therefore improved SiGe bipolar yield is obtained.

A drawback of the known method is that it complicates the method of manufacturing a bipolar transistor, as it requires several additional process steps. In this way also the cost are increased.

Therefore, it is an object of the present invention to provide a method by means of which bipolar transistors can be made while on the one hand bridging between silicide regions is avoided while on the other hand the method is simple and cheap.

To achieve this, in accordance with the invention, a method of the type mentioned in the opening paragraph is characterized in that the means to prevent bridging of the silicides to be formed comprises that the side face of the stack is structured in such a way that the distance between the upper surface of the remaining part of the semiconductor layer and the upper surface of the second region of the semiconductor body along the surface of the side face of the stack is made longer than the total thickness of the insulating layer and the semiconductor layer. The invention is based on the recognition that increasing the length of a path along the side face of the stack already is sufficient to avoid the occurrence of the bridging problem. The invention is further based on the recognition that such increased path length can be created in a simple manner by structuring the profile of the stack – which in the method of prior art is made rectangular – such that so to say the slope of the profile is changed by which the length of said path is increased. Both a positive slope in the side face of the remainder of the insulating layer as well as a negative slope in the side face of the remainder of the semiconductor layer will result in an increased path along the side face of the stack of both layers, which will result in avoidance of the bridging problem. In case of a negative slope also (some) shadow operation which will occur during deposition of the metal layer required for forming the silicides will be advantageous in this respect. Finally, the invention is based on the recognition that a structuring as envisaged is possible using merely the etching steps which are needed anyway to remove parts of the insulating layer and the semiconductor layer in a specific manner which will be described hereinafter. Thus, the method according to the invention does not or at least hardly makes the method more complicated. The method thus also is cheap.

In a first preferred embodiment of method in accordance with the invention, the removal of the semiconductor layer and the insulating layer in the second region is done by an etching process such that the side face of the remaining part of the insulating layer is made convex and extends viewed in projection outside the remaining part of the

semiconductor layer. The convex part may be substantially linear but this is not necessary. Such a positive outward slope of the side face of the remainder of the insulating layer is easily obtained if a dry etching process is used for removing part of the insulating layer that is based on the chemistry of fluor and carbon. The carbon may be provided by a photoresist layer which will be present during the etching process as a mask. The fluor compound(s) may be added to the plasma. In such a process polymers of fluor and carbon will deposit at the edges in the bottom of a hole to be etched in the insulating layer. Subsequently, the same etching process may remove them. However, as a results of these phenomena the remainder of the insulating layer will taper outwardly with a slope of e.g. about 45 degrees. In this way the path length along the side face of the stack is increased by which the bridging problem is avoided. The slope may be smaller than 45 degrees for the envisaged effect, however such a small slope also has disadvantages. A preferred value of the slope lies between 30 and 60 degrees.

In a second preferred embodiment of a method in accordance with the invention the removal of the semiconductor layer in the second region is done by an etching process such that the side face of the remaining part of the semiconductor layer is made concave end extends viewed in projection inside towards the remaining part of the insulating layer. In this way also the path length along the side face is increased in a simple manner. Moreover, there is a shadow effect that may be advantageous in avoiding the bridging problem. Such a profile of the remainder of the semiconductor layer may e.g. be obtained in that a first upper part of the semiconductor layer is etched by using an anisotropic dry etching process and a second, lower part of the semiconductor layer is etched using an isotropic etching process.

In an advantageous modification of method in accordance with the invention the semiconductor layer is provided with a doping profile such that a lower part of the semiconductor layer has a high doping level and an upper part of the semiconductor layer has a low doping level and the difference in doping level between the parts is used to form the desired concave side face of the remaining part of the semiconductor layer. Such a difference may result in a different etching speed in the same, e.g. wet, etching agent, whether or not combined with the addition of light to the surface to be etched. Also in case a pn-junction is introduced in the semiconductor layer, selective etching of part of the side face of the remainder of the semiconductor layer may be obtained. Afterwards, the pn junction may be removed by etching or overdoping, e.g. by ion implantation of suitable doping atoms.

One attractive variation on the above method is that after an anisotropic etching process of the semiconductor layer, the side face of the remaining part of the semiconductor layer is thermally oxidized and subsequently the resulting oxide is removed by a wet etching agent based on HF. The above mentioned difference in doping level will result in a different depth of oxidation of the side face of the remainder of the semiconductor layer. After removal of said (silicon) oxide on the side face, a notch will result at the lower part of the remainder of the semiconductor layer, providing the required path lengthening and providing a shadow effect. The preferably not yet etched insulating layer will protect the semiconductor body during this etching step. Subsequently, the insulating layer is partly etched, preferably by means of a dry, anisotropic etching process.

Preferably, the remainder of the insulating layer and the remainder of the semiconductor layer and a layer on top thereof are used as a mask for doping the second region of the semiconductor body. In this way an enhanced doping level of said region, which will later on serve as a connection region for the base of the bipolar transistor, is easily provided. High speed and low dissipation of the device are improved in this way.

It is preferred that the base is formed by providing the semiconductor body with a doped further semiconductor layer which locally borders on a monocrystalline part of the semiconductor body, thereby forming a first semiconductor region which is monocrystalline and which constitutes the base of the transistor and which further semiconductor layer borders at locations outside the base on a non-monocrystalline part of the semiconductor body thereby forming a second semiconductor region which is not monocrystalline and which constitutes a connection region of the base and the collector is formed by a further part of the semiconductor body situated below the base. Such process is particularly suitable for the manufacturing of very high-speed heterojunction bipolar transistors with e.g. SiGe in the base.

Finally, the invention comprises a semiconductor device with a bipolar transistor with a base, an emitter and a collector in a semiconductor body of silicon and having above the emitter an insulating region with a window which is filled with a semiconductor region of silicon which extends over the surface of the insulating region and with silicides formed on top of the silicon region and on top of the semiconductor body on both sides of the insulating region, characterized in that the side face of the stack formed by the insulating region and the silicon region is structured in such a way that the distance between the upper surface of the silicon region and the surface of the semiconductor body along the surface of the side face of the stack is made longer than the total thickness of the

insulating region and the silicon region. Such a device which is characterized by a slope of the side face of the region above the base / emitter which deviates from a direction perpendicular to the layer structure, has the above mentioned advantages and may be obtained with a high yield by a method according to the invention due to the fact that such a slope results in avoidance of the above explained bridging problem. Both positive and negative slopes are suitable. The slope may be in the insulating or in the silicon region (or both).

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawings:

Figs 1 through 11 are diagrammatic, cross-sectional views, at right angle to the thickness direction, of a semiconductor device with a bipolar transistor at successive stages in the manufacture using a first embodiment of a method in accordance with the invention;

Figs 12 through 15 are diagrammatic, cross-sectional views, at right angle to the thickness direction, of a semiconductor device with a bipolar transistor at successive relevant stages in the manufacture using a second embodiment of a method in accordance with the invention;

Figs 16 through 19 are diagrammatic, cross-sectional views, at right angle to the thickness direction, of a semiconductor device with a bipolar transistor at successive relevant stages in the manufacture using a third embodiment of a method in accordance with the invention.

The Figures are diagrammatic and not drawn to scale, particularly the dimensions in the thickness direction being exaggerated for clarity. Semiconductor regions of the same conductivity type are generally hatched in the same direction. Like reference numerals refer to like regions whenever possible.

Figs 1 through 11 are diagrammatic, cross-sectional views, at right angle to the thickness direction, of a semiconductor device with a bipolar transistor at successive stages in the manufacture using a first embodiment of a method in accordance with the invention. The starting point (see fig. 1) is formed by a p-type silicon substrate 11 that is provided with an epitaxial.layer 33 of n-type silicon which is moderately doped. Before the deposition of the

layer 33 an n+ type buried region 3A1 is formed by means of ion implantation. In the surface of the semiconductor body 100, isolation regions 8 are formed of silicondioxide in this example as LOCOS (= LOCal Oxidation of Silicon) regions 8. By means of diffusion a connection region 3A2 is made for connection of the collector 3 of the transistor to be formed. Subsequently a thermal oxide layer 9 is formed on the (cleaned) surface of the semiconductor body 100 and on top thereof a thin polycrystalline silicon layer 4 is deposited thereon. With the aid of photolithography a mask 20, e.g. of silicondioxide is patterned on top of the poly-silicon layer 4. In the latter (see figure 2) a window is opened by means of etching at the location of the active area of the bipolar transistor to be formed. It is to be noted that in stead of a poly silicon layer 4 also a layer of poly silicon on silicon nitride may be used or only a layer of silicon nitride.

Then (see figure 3) the oxide layer 9 is removed inside the window. After removal of the mask layer 20 (see figure 4) a silicon layer 12 is deposited by means of epitaxy and CVD (= Chemical Vapor Deposition) on top of the surface of the semiconductor body 100. The silicon layer 12 is monocrystalline at the active area of the transistor and will form the base 1 of the transistor. For that purpose the layer 12 is provided during growth with a p-type doping spike. Also a thin sublayer – not indicated separately in the drawing – containing a SiGe mixed crystal may be provided which is made so thin that no misfit dislocations are formed. Above the isolation regions 8 the silicon layer 12 is polycrystalline and will form part of a connection region 1A of the base 1.

On top of the silicon layer 12 (see fig. 5) a 20 to 200 nm thick silicondioxide layer 13 is deposited by means of CVD. At the location were the emitter of the transistor is to be formed a small window is opened in the insulating layer 13 by means of photolithography and etching. Subsequently, a polycrystalline silicon layer 14 is deposited by means of CVD on top of the surface of the semiconductor body 100 which fills the opening in the insulating layer 13 and extends laterally over said layer. A mask 50, here of photoresist, is patterned above the structure, the width thereof being e.g. 0,5 μm, which is about 100 to 200 nm outside the emitter area whereas the width of the opening in insulating layer 13 below the mask 50 is e.g. about 0,3 μm but could be as small as about 100 nm in a very advanced device. It is to be noted that layer 13 also may comprise a stack of different dielectric layers in view of an etch stop function. It is further noted that the bridging problem which above has been defined and which is avoided in the present invention, may in particular occur if the thickness of the dielectric layer 13 is less than about 60 nm.

Then (see fig. 6) the silicon layer 14 is removed outside the mask 50 by means of etching, e.g. dry etching. Subsequently, the insulating layer 13 outside the mask 50 is removed by dry-etching as well. The process is based on the chemistry of compounds of fluor and carbon. Therefore (see figure 7) the silicondioxide layer 13 will under suitable etching conditions, taper outside the mask 50 gradually toward a thickness of zero. With the aid of a mask 70, which is typically at least 1 µm wide and extends 0,2 to 0,5 µm outside the active region, the layers 9,4 and 12 are removed outside the active area of the transistor to be formed. In between the stages of figures 5 and 6, the remaining parts of the insulating layer 13 and the silicon layer 14 and the mask layer 50 on top thereof are used to implant additional p-type impurities in the silicon layer 12 outside this structure. The resistance of the base connection region 1A is decreased in this way.

After the layers 9,4,12 have been removed outside the active area of the transistor to be formed (see fig. 8) a metal layer 16, here of titanium, is deposited on the structure 100. The metal layer 16 also could be a stack of different metal layers. During a short heat treatment at 720 degrees Celsius (see fig. 9) the metal layer 15 reacts with the silicon parts to which it is exposed to form silicides 17 at the locations of the base connection region 1A, the collector connection region 3A2 and at the location of the poly-silicon above the emitter to be formed. Next (see fig. 10) the parts of the metal layer 16 that did not react with silicon are removed by means of etching. During a subsequent heat treatment at 850 degrees Celsius, the silicides 17 are transformed from a monosilicide towards a disilicide, the latter having the lower sheet resistance. At the same time emitter 2 is formed by outdiffusion of impurities from the remaining part of the silicon layer 14 into the base layer 12. For this reason the poly-silicon layer 14 is n-type doped during its deposition as the present example deals with a npn bipolar transistor. The emitter may also be formed in a separate RTA (= Rapid Thermal Anneal) at e.g. 1000 degrees Celsius, before the silicidation takes place.

Thanks to the presence of the tapered region in the insulating layer 13 outside the remaining part of the silicon layer 14, the distance between the remaining part 14 of polysilicon and he surface of silicon layer 112 is increased compared to the case wherein the side face of the remaining part of the insulating layer 13 would run perpendicular to the layer structure. In this way, bridging of the silicides 17 formed on top of the remaining part of the silicon layer 14 and formed on top of the silicon layer 12 is avoided during both silicide forming steps described before.

Finally (see figure 11) an insulating layer 18, e.g. of silicondioxide is deposited on the surface of the semiconductor body 100. It is provided with openings in

which connection conductors 19 are formed. After separation of the device 10 from a wafer in which it is formed, it is suitable for use.

Figs 12 through 15 are diagrammatic, cross-sectional views, at right angle to the thickness direction, of a semiconductor device with a bipolar transistor at successive relevant stages in the manufacture using a second embodiment of a method in accordance with the invention. As many of the manufacturing steps are the same as in the previous example, these steps will be not repeatedly described. Only the relevant steps will be discussed. After the situation of figure 5 has been reached, the manufacture proceeds as shown in figure 12. In this example the etching of the poly-silicon layer 14 is done in such a way that the remaining part of the silicon layer 14 shows a sideface with a negative slope, i.e. the sideface tapers inwardly and downwardly towards the interface with the insulating layer 13 below the mask 50.In this example this is obtained by etching the silicon layer 14 in two etching steps: a first etching step based on Cl2 chemistry for obtaining anisotropy and based on HBr for obtaining sidewall passivation followed by a second isotropic etching step based on fluor chemistry, e.g. by using SF6. Subsequently, the insulating layer 13 is removed using a anisotropic etching process resulting in a sideface running perpendicular to the layer structure: see figure 13. The stages of figure 13, 14 and 15 correspond with those of figures 7, 8 and 10, and the stage of figure 9 is not shown separately in this example.

Also in this example the length of the path along the side face of the stack formed by the remaining parts of the insulating layer 13 and the silicon layer 14 is of increased length. Thus bridging of silicides 17 formed on top of layers 12 and 14 is avoided. The shadow effect of the negative slope may be observed in figure 14 and has the advantage that there will be little or even no metal deposited on the side face of the poly silicon.

Figs 16 through 19 are diagrammatic, cross-sectional views, at right angle to the thickness direction, of a semiconductor device with a bipolar transistor at successive relevant stages in the manufacture using a third embodiment of a method in accordance with the invention. It is again referred to the first example for most of the manufacturing steps. The in this example relevant step corresponding with figure 6 is shown in figure 16. The remaining part of the silicon layer 14 has in this example two different doping levels on both sides of the dashed line: a lower part 14A is provided with a high doping level whereas the upper part 14B is provided with a low doping level. After removal of the silicon layer 14 outside the mask 50 (see figure 17) the side face of the remaining part of the silicon layer 14 is thermally oxidized so as to form oxide region 40. As the oxidation rate of silicon is higher at a higher doping level, the oxide region 40 has a stepped profile as shown in figure 17.

After a dip in an aqueous solution of HF, said oxide region 40 is removed and the result is (see figure 17) a remaining part of the silicon layer 14 having a notch just below the remaining part of the insulating layer 13.

Here again both path lengthening and shadow effect occur at the sideface of the stack of the remaining parts of the insulating layer 13 and silicon layer 14 by which again the occurrence of bridging during silicide 17 formation is prevented. The stages of figures 18 and 19 correspond with those of figures 9 and 10, the situation of figure 9 being again not separately shown.

Finally, it should be noted that were the layer(s) being deposited in and around the emitter window (in the dielectric layer) are shown in the drawing as having a planar top surface, this surface will be in reality not planar but will have a ditch / notch at the location of the window. The invention is also based on the recognition that such a ditch / notch makes the use of (outside) spacers less feasible.

The invention is not limited to the above-mentioned examples, and within the scope of the invention many modifications and variations are possible to those skilled in the art. For example, composition and thicknesses for the different (semiconductor) layers or regions may be selected which differ from those mentioned in the examples. It is also possible to use different deposition techniques, such as MBE (= Molecular Beam Epitaxy) or sputtering of PVD (Physical Vapor Deposition).

The method according to the invention may be very well applied to a more complex device than a single bipolar transistor. The device may comprise a number of different active or passive electronic or semiconductor components. The transistor may also form part of a BI(C)MOS IC (= Bipolar (Complementary) Metal Oxide Semiconductor Integrated Circuit).